REMARKS

The present Amendment amends claims 17, 18, 21-23, 27, 28, 31, 32 and 35-37 and leaves claims 19, 20, 24-26, 29, 30, 33, 34 and 38-40 unchanged. Therefore, the present application has pending claims 17-40.

Claims 17-40 stand rejected under 35 USC §102(a) as being anticipated by DeGroot (U.S. Patent No. 4,766,564). This rejection is traversed for the following reasons. Applicants submit that the features of the present invention as now more clearly recited in claims 17-40 are not taught or suggested by DeGroot whether taken individually or in combination with any of the other references of record. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

Amendments were made to each of the claims particularly the independent claims so as to more clearly describe that the present invention is directed to a processor which implements a super scalar technique wherein a plurality of instructions are fetched at a time from memory and the plurality of fetched instructions are executed in parallel. These features of the present invention now recited in the claims are described, for example, on page 8, lines 9-10 and page 11, lines 21-22 of the present application.

The above described features of the present invention now more clearly recited in the claims, particularly with regard to the claims being directed to processors implementing a super scalar technique, are not taught or suggested by any of the references of record whether taken individually or in combination with

each other. Specifically, these features of the present invention now more clearly recited in the claims are not taught or suggested by DeGroot.

DeGroot teaches a data processing system having multiple floating point arithmetic units, two put away buses and bypass buses which operate together in a manner so as to execute a number of floating point arithmetic operations in a given cycle of operation. However, in DeGroot although the multiple floating point arithmetic units operate in parallel the fetching of instructions to be executed are performed sequentially. Specifically, DeGroot teaches, for example, in col. 3, lines 9-14 that:

> "the instruction register 26 sequentially receives instructions from the central memory 32 and executes them. As the instructions are executed, floating point numbers are transferred between the register file 8 and memory 32 and certain operations on these numbers are initiated within the arithmetic unit".

The present invention differs substantially from that taught by DeGroot being that the present invention provides within each processor means for fetching from memory a plurality of instructions at a time. Fetching a plurality of instructions at a time differs from the sequential fetching operation as taught by DeGroot.

The present invention further provides that the arithmetic unit executes a plurality of fetched instructions in parallel. Thus, in the present invention plural instructions are fetched and plural instructions are executed in parallel. Such features are clearly not taught or suggested by DeGroot. In DeGroot, the instructions are executed sequentially and floating point calculations based on floating point numbers are calculated in parallel. Therefore, in DeGroot, the

instructions are executed sequentially contrary to the parallel execution of instructions recited in the claims.

Thus, DeGroot fails to teach or suggest means for fetching from memory a plurality of instructions at a time as recited in the claims.

Further, DeGroot fails to teach or suggest a plurality of arithmetic operation units operable to execute the plurality of instructions fetched from the memory in parallel as recited in the claims.

Therefore, as is quite clear from the above, the features of the present invention as now more clearly recited in the claims are not taught or suggested by DeGroot whether taken individually or in combination with any of the other references of record. Accordingly, reconsideration and withdrawal of the 35 USC §102(a) rejection of claims 17-40 as being anticipated by DeGroot is respectfully requested.

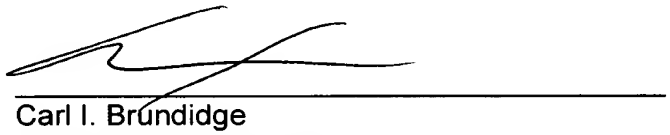
The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the reference utilized in the rejection of claims 17-40.

In view of the foregoing amendments and remarks, applicants submit that claims 17-40 are in condition for allowance. Accordingly, early allowance of claims 17-40 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C., Deposit Account No. 50-1417 (500.28166CX2).

Respectfully submitted,

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.



Carl I. Brundidge
Registration No. 29,621

CIB/jdc
(703) 684-1120